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CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8) Applicant(s): Divakaruni et al.			Docket No. FIS920030274US1
Serial No. 10/707,388	Filing Date 12/10/2003	Examiner Steven J. Fulk	Group Art Unit 2891

Invention: **SILICIDE RESISTOR IN BEOL LAYER OF SEMICONDUCTOR DEVICE AND METHOD**

I hereby certify that this **Pre-Approval Brief Request for Review with Attachments in 7 pages**
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on **February 8, 2006**
(Date)

Jennifer L. Kelly
(Typed or Printed Name of Person Signing Certificate)

Jennifer L. Kelly
(Signature)

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PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) FIS920030274US1	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope address to "Mail Stop AF, Commissioner Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on February 8, 2006 Signature Jennifer L. Kelly Typed or printed name Jennifer L. Kelly	Application Number 10/707388	Filed 12/10/2003
	First Named Inventor Divakaruni et al.	
	Art Unit 2891	Examiner Steven J. Fulk

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 40,398.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. _____

Signature

Spencer K. Warnick
Typed or printed name

518-449-0044
Telephone number

February 8, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Divakaruni et al.

Serial No.: 10/707,388

Filed: 12/10/2003

Title: SILICIDE RESISTOR IN BEOL LAYER OF SEMICONDUCTOR DEVICE AND METHOD

Conf. No.: 1387

Art Unit: 2891

Dkt. #: FIS920030274US1 (IBMF-0032)

Examiner: Fulk, Steven J.

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicants request a panel of experienced examiners perform a detailed review of appealable issues for the above-identified patent application pursuant to the Pre-Appeal Brief Conference Pilot Program. Notice of Appeal has been filed together with this Request.

Applicants submit that the above-identified application is not in condition for appeal because the Office has failed to establish a *prima facie* case of obviousness due to errors in facts and in law. Claims 1-20 are pending in this application, among which claims 1-11 are withdrawn from consideration.

In the final Office Action (OA), claims 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al. (US Publication No. 2003/0183880), hereinafter "Goto," in view of Wolf, *Silicon Processing for the VLSI Era*, 1986, Volume I, pages 387 and 400, hereinafter "Wolf 1986," and Wolf, *Silicon Processing for the VLSI Era*, 1990, Volume II, page 146, hereinafter "Wolf 1990." Applicants submit that this rejection is clearly not proper and without basis for the reasons stated below.

With respect to independent claims 12 and 20, for example, Applicants submit that the suggested combination of the cited prior art does not disclose or suggest, *inter alia*, "a silicide section positioned in one of a plurality of back-end-of-line (BEOL) layers[,] wherein the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers[.]" (Claim 12; similarly in claim 20). As the Office admits, Goto does not disclose or suggest this feature. (OA at 2). Applicants submit that Wolf 1986 and Wolf 1990 also do not disclose or suggest "a silicide section positioned in one of a plurality of back-end-of-line (BEOL) layers[.]" (Claim 12). The Office asserts, however, that "the resistor could be formed in any layer of the semiconductor device, including BEOL layers[.]" (OA at 3). Applicants respectfully traverse this assertion because there is no suggestion or motivation to modify the two Wolf references in a manner to obtain the above-referenced feature. Wolf 1990 attempts to use the group VIII metals for "self-aligned ohmic contacts and local interconnects to silicon." (Wolf 1990 at 146). As is known in the art, self-aligned ohmic contacts and local interconnects to silicon are in the first metal layer, which is by definition not one of a plurality of BEOL layers, as BEOL layers are formed on a semiconductor wafer in the course of device manufacturing following the first metallization.

In the Advisory Action of 1/20/06 (AA), the Office asserts that "the reference separately defines silicon contacts from interconnects, where interconnects are used for BEOL layers." (AA at 2, citing Wolf 1986 at 400.) Applicants respectfully traverse this assertion because the Office misinterprets Wolf 1986. Wolf 1986 discloses "gate interconnections", instead of "interconnects used for BEOL layers" as the Office asserts. (Wolf 1986 at 400, ¶ 1). As is known in the art, a "gate interconnection" is in the first metal layer, not one of a plurality of

BEOL layers. In view of the foregoing, the cited prior art does not disclose or suggest "a silicide section positioned in one of a plurality of back-end-of-line (BEOL) layers[.]"

In addition, Wolf 1990 only discloses that "[a]ll of the group VIII metals react with Si at 600°C or less" (Wolf 1990 at 146), and Wolf 1986 only discloses that "silicides form [on Tungsten] at temperature > 600 °C" (Wolf 1986 at 400). Such disclosures of the silicidation temperatures of the metals, without more, do not teach or suggest the claimed features. For example, both Wolf references do not disclose or suggest a damaging temperature of a plurality of BEOL layers, nor that a silicide section has a silicidation temperature less than a damaging temperature of a plurality of BEOL layers. Applicants submit that the absolute value of 600°C or less disclosed in Wolf 1990 is not equivalent to the relative temperature characteristic in the claimed invention, i.e., a silicidation temperature less than a damaging temperature of the plurality of BEOL layers. Applicants submit that the Office is using the hindsight teachings of the claimed invention to modify the Wolf references to obtain "a silicidation temperature less than a damaging temperature of the plurality of BEOL layers." (Claim 12).

In the Office Action, the Office asserts that "the silicidation temperature that ... are [*sic.*] less then a damaging temperature of a plurality of BEOL layers are defined in applicant's specification as 600°C or less[.]" (Office Action at pages 3-4). Applicants respectfully disagree because the specification of the current application, e.g., ¶ 0020, provides the anneal temperature ranges of some illustrative examples of the metals that may be deposited on one of a plurality of BEOL layers, but does not define a damaging temperature of a plurality of BEOL layers as 600°C or less, and do to limit the scope of the invention, including the damaging temperatures. Rather, the specification of the claimed invention clearly describes that "[f]or alternative BEOL

wiring schemes that allow higher temperature processing, there are other material options for first metal 40[.]" (¶ 0021).

In the AA, the Office asserts that "[i]f this [i.e., the specification provides examples instead of a definition of damaging temperature] is the case, the phase 'less than a damaging temperature of the plurality of BEOL layers' is not defined in the specification[,] [and] [i]ssues of enablement under U.S.C. 112 1st Paragraph would then arise[.]" (AA at 3). Applicants disagree because the Office confuses the broadness of the claims with a failure to meet the enablement requirement. The examples described in the specification are enough to enable a person with ordinary skill in the art to implement the invention without undue experimentation. However, the scope of the invention is not limited by the examples. In addition, the phrase "less than a damaging temperature of the plurality of BEOL layers" in the claimed invention is definite because for a specific BEOL layer, there is a specific, ascertainable damaging temperature. Here again, Applicants submit that the Office confuses the broadness of the claims with a failure to meet the 35 U.S.C. 112, second paragraph requirement.

In the Office Action, the Office asserts that "interconnects are, by definition, part of the back-end-of-line process." (OA at 3). Applicants disagree because FEOL layers also include interconnects. Moreover, Wolf 1990 only expects "interconnects to silicon" (Wolf 1990 at 146), not interconnects between BEOL layers because BEOL layers may include metal layers and dielectric layers, but do not include silicon. In view of the foregoing, the suggested combination does not disclose or suggest, *inter alia*, "the silicide section has a silicidation temperature less than a damaging temperature of the plurality of BEOL layers."

Furthermore, Applicants submit that there is no suggestion or motivation to combine the cited references. Wolf 1990 and Wolf 1986 only expect to use the group VIII metals for forming

"contacts metals to Si", but not for forming a resistance element. (Wolf 1990 at 146). As such, there is no motivation or suggestion to adopt the teachings of the Wolf references into Goto to form the resistance element. The Office can obtain suggestion or motivation to combine the two Wolf references with Goto only from the hindsight teachings of the claimed invention.

In the AA, the Office asserts that "the resistivities of the silicide interconnect are equivalent to the silicide resistivities claimed by the applicant, and thus the structural limitations of the silicide section are anticipated by Wolf." (AA at 2, inner citation omitted). Applicants respectfully disagree because the Wolf references only disclose physical characteristics of the VIII metals, i.e., low resistivities and silicidation temperatures, but not structural limitations of a resistance element of the claimed invention. In addition, the claimed invention does not claim "silicide resistivities", but claims, *inter alia*, a resistor including "a silicide section positioned in one of a plurality of back-end-of-line (BEOL) layers[.]" (Claim 12). The Wolf references do not anticipate such structural limitations.

In view of the foregoing, Applicants submit that the Office has failed to state a *prima facie* case of obviousness, and this application is not in condition for appeal and should either be allowed as is, or re-opened for further prosecution.

Respectfully submitted,

Date: 2/8/06

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